Remarks

Claims 1, 9, 17, and 25 have been amended. Claims 10 and 26 are cancelled herein and claims 4, 13, 20 and 29 were previously cancelled. Following the above amendments, claims 1-3, 5-9, 11-12, 14-19, 21-25, 27-28, and 30-32 are pending in this application. The Examiner has rejected claims 1, 3, 6-12, 15-17, 19, 22-28, 31, and 32 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,774,647 to Raynham et al (hereinafter "Raynham") in view of U.S. Patent No. 5,588,112 to Dearth et al (hereinafterr "Dearth"), and further in view of U.S. Patent No. 6,125,392 to Labatte et al (hereinafter "Labatte"). The Examiner has also rejected claims 2, 5, 14, 18, 21, and 30 under 35 U.S.C. § 103(a) as being obvious over Raynham in view of Dearth and Labatte, and further in view of Brisse et al. (WO 99/05599) (hereinafter "Brisse"). Applicant respectfully traverses the Examiner's rejections.

A. Independent Claims 1, 9, 17 and 25

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The combination of Raynham, Dearth, and Labatte fails to teach or suggest all the claim limitations of independent claims 1, 9, 17, and 25. Specifically, the combination fails to teach or suggest that the means for detecting an error are operable to generate an exception within the central processing unit, with the central processing unit (or system) having an assigned exception vector. In the present invention, a memory failure in any module generates an

exception when the CPU of the system tries to access a specific memory location within one of the memory modules which malfunctions. (Spec., page 13, line 13) Because the CPU is not able to access the location in the malfunctioning module, an exception is generated, and the CPU has an assigned trap or exception vector for such a memory access. (Spec., page 13, line 15) The BIOS then has a routine for this assigned exception vector, the assigned exception vector making it possible for the BIOS to recognize and act upon the exception.

The Examiner does not assert that Dearth or Labatte teaches this limitation. Labatte does not discuss exceptions and interrupts. Dearth discusses interrupts, but fails to teach or suggest that a means for detecting a memory error is also operable to generate an exception within a central processing unit, and also fails to discuss the specific requirement of an exception vector. The Examiner points to Raynham as (not explicitly) teaching this limitation, formerly in dependent claims 10 and 26. (Office Action, p.5) The cited portion of Raynham discusses that when an I/O bridge and memory controller detects an error, an interrupt is generated to the main processor. (Raynham, 10:4-18) However, Raynham fails to teach or suggest that an exception is generated within a central processing unit having an **assigned exception vector.** At best, Raynham teaches that an interrupt is generated, but no mention is made of an assigned exception vector that the BIOS may recognize in order to execute a routine. In fact, in Raynham, the processor must send an I2C message through a baseboard interface to a system management controller, which then forwards the I2C message back through the baseboard interface to a memory controller in order to log an error message. (Raynham, 10:4-18) In contrast, in the present invention, the central processing unit has an **assigned** trap or **exception vector** for when a memory access to a memory module fails, and the BIOS comprises a respective routine for error documentation for this **assigned exception vector**. (Spec., page 13, line 13) Thus, the

assigned exception vector allows the BIOS to recognize and act upon the exception occurring. Raynham fails to teach or suggest a means for detecting an error operable to generate an exception within the central processing unit, with the central processing unit (or system) having an **assigned exception vector.** Because Dearth and Labatte fail to remedy this deficiency, the combination fails to teach this element, as well.

A prima facie case of obviousness has not been established because the combination of Raynham, Dearth, and Labatte does not teach or suggest all of the claimed elements of independent claims 1, 9, 17, and 25. Thus, the rejection of claims 1, 9, 17, and 25 under 35 U.S.C. 103(a) should be withdrawn.

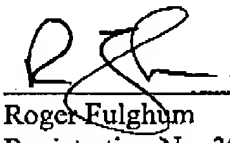
B. The Rejection of Dependent Claims 2, 3, 5-8, 11-12, 14-16, 18, 19, 21-24, 27-28 and 30-32

The rejection of dependent claims 2, 3, 5-8, 11-12, 14-16, 18, 19, 21-24, 27-28 and 30-32 will not be discussed individually herein, as each of these claims depends, either directly or indirectly, from an otherwise allowable base claim.

Conclusion

Applicant respectfully submits that the pending claims 1-3, 5-9, 11-12, 14-19, 21-25, 27-28, and 30-32 of the present invention, as amended, are allowable. Applicant respectfully requests that the rejection of the pending claims be withdrawn and that these claims be passed to issuance.

Respectfully submitted,



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